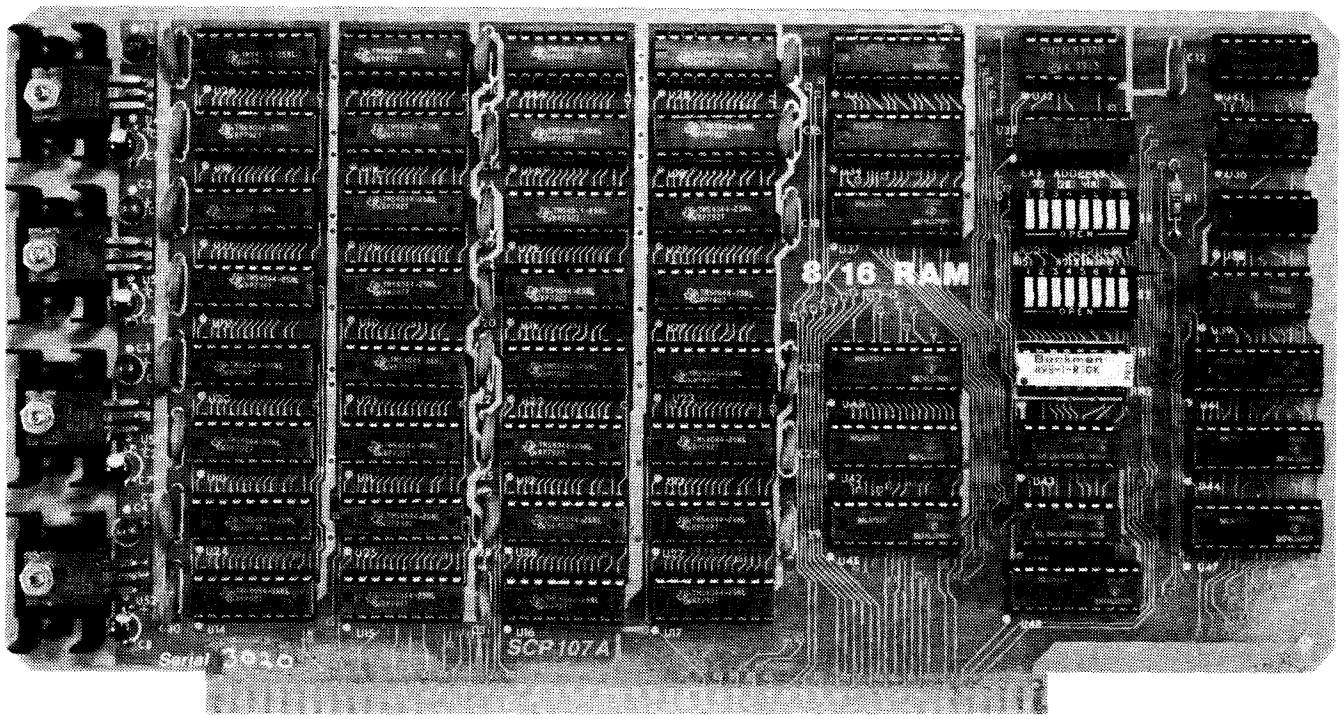
Instruction Manual

Model SCP-107



8/16 RAM

16K RAM for Both 8-bit and 16-bit S-100 Systems

The 8/16 RAM is a fully static, high performance memory card which will store 16K bytes of information and can be used with either 8-bit or 16-bit wide systems. Data path width is dynamicly selected by the board depending upon the state of the sXTRQ* signal as specified by the IEEE Proposed Standard for the S-100 Bus.

The board was designed to operate with the Seattle Computer Products 8086 CPU board with the CPU using clock speeds to 8 Mhz. The memory board uses "extended addressing" allowing it to be located within a 16 megabyte addressable range.

The board is characterized by the same high noise immunity type design employed in the company's highly successful 8-bit PLUS and APEX memory cards. Reliability of these latter boards has been demonstrated to exceed 98% for the first year of operation with recent data suggesting current production boards will have reliabilities exceeding 99%.

Seattle Computer Products, Inc.
1114 Industry Drive, Seattle, WA. 98188
(206) 575-1830

Rev. A

Configuring the Board

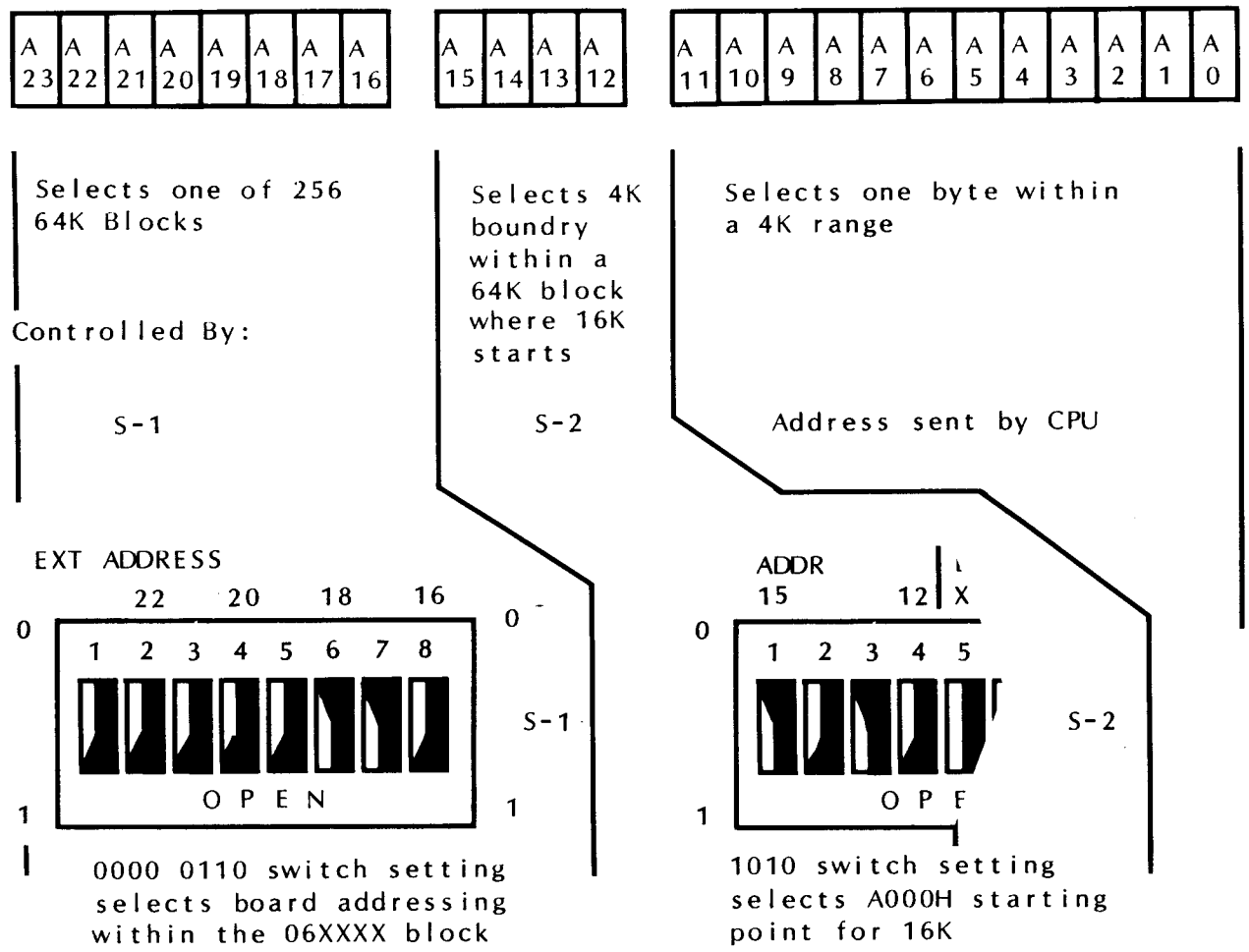
To configure the board to operate in your system, only three items must be considered:

1. Where do you want to address it?
2. Are you going to use the memory card with a 16-bit processor?
3. Do you want to use the PHANTOM* signal to disable the board?

Each of these considerations will be discussed in turn.

ADDRESSING THE BOARD

This board has provision for "extended addressing". That is, the board can be addressed for 16K within a range of 16,777,216 bytes. A-0 through A-15 are used to define an address within a 64K block. A-16 through A-23 are used to define an address as being in one out of 256 64K blocks.



Extended addressing replaces the older bank select schemes which turn memory boards on and off through the use of an output port.

SELECTED 16K WITHIN 64K BLOCK

SWITCH 2

Switch Segment				0000 TO 0FFF	1000 TO 1FFF	2000 TO 2FFF	3000 TO 3FFF	4000 TO 4FFF	5000 TO 5FFF	6000 TO 6FFF	7000 TO 7FFF	8000 TO 8FFF	9000 TO 9FFF	A000 TO AFFF	B000 TO BFFF	C000 TO CFFF	D000 TO DFFF	E000 TO EFFF	F000 TO FFFF
1	2	3	4																
0	0	0	0																
0	0	0	1																
0	0	1	0																
0	0	1	1																
0	1	0	0																
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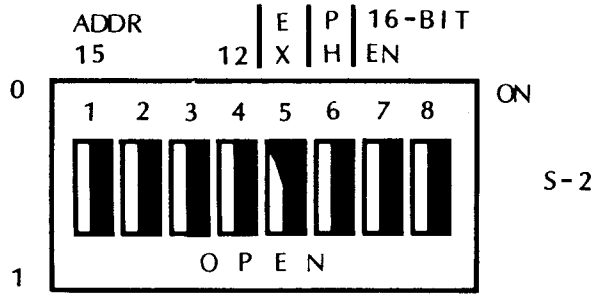
EXTENDED ADDRESS NOT USED

If your system does not use extended addressing, the entire extended addressing circuitry may be disabled by "turning off" switch segment 5 of S-2.



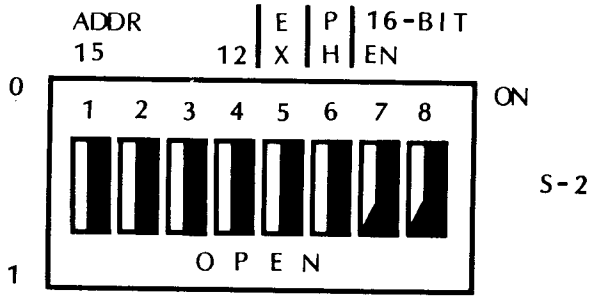
Extended addressing is shown "turned off" on S-2. The board now disregards any information conveyed by the extended address lines A-16 through A-23.

16-BIT ENABLE

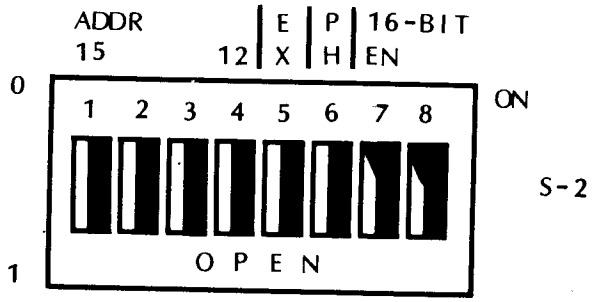
The S-100 bus lines 58 and 60 are used for sXTRQ* and SXTN*, respectively the Sixteen Request and Sixteen Acknowledge signals.

If you are using this memory card with our 8086 CPU, you will want to have these lines connected so the memory card can do 16-bit transfers. However, if you are using this card with an older 8-bit system, there may be a conflict of use for bus lines 58 and 60. If a conflict exists, disconnect these lines by switching both segments 7 and 8 of S-2 to the "off" position.

If there is no conflict with these bus lines, segments 7 and 8 may be in either position. The memory card will work 8-bits wide with 8-bit CPUs.



sXTRQ* and SXTN* Enabled



sXTRQ* and SXTN* Disabled

PHANTOM

Some systems require the use of a PHANTOM* signal to disable memory while a ROM, co-located in the same address space as memory, is being read. This PHANTOM* signal may be used with this board.

Our 8086 CPU was designed to be compatible with existing 8-bit memories. To allow use of this existing memory, which does not have extended addressing, the CPU has the capability of outputting a a PHANTOM* signal whenever memory above the lowest 64K is being addressed. This PHANTOM* signal can be used to disable these older memories when extended addressing is being used.

The PHANTOM* signal line should not be connected on the 8/16 if the above mode of operation is selected on our 8086 CPU.

* Indicates an active low signal.

Theory of Operation

The 8/16 RAM operates differently from 8-bit only memory cards. It must function in both 8-bit mode and the 16-bit mode. That is, it must be capable of reading and writing data which can be either 8 bits wide or 16 bits wide.

In the 8-bit mode, it operates similar to the way that previous 8-bit memories have functioned. Data sent from the CPU to be written into memory is sent over the Data Out lines of the bus. Data to be read by the CPU is transferred from memory over the Data In lines of the bus. MWRITE and pDBIN are the two principal control signals sent by the CPU to the memory board to indicate whether a read or write operation is required.

However, to accommodate the new 16-bit processors which require 16-bit wide data paths, the IEEE S-100 Bus Standard Committee agreed to change the two data paths -- the Data Out Bus and the Data In Bus. Where previously each had been "one-way", now they were to become "two-way". When a 16-bit read was called for, data from 16-bit memories would be sent to the CPU over both the Data In and Data Out busses. A write command would transfer the data back to the memory card over the same two busses. In this latter case, the data would move over the busses in the opposite direction.

If only 16-bit transfers were considered, the same two control signals -- MWRITE and pDBIN -- could be used to switch these two busses from "data in" to "data out". However, if we were to use only 16-bit transfers, this would require all peripherals to also be 16-bits wide. This would obsolete all existing peripherals. In addition, since all of the modern processors, the 8086, Z8000, and 68000 also make 8-bit transfers, a 16-bit only system would be using only part of the processor instruction set.

The 8/16 RAM operates in both the 8-bit and 16-bit modes. In addition to the normal read/write control signals of MWRITE and pDBIN, a new one is generated by modern CPUs to indicate whether the data being transferred is 8-bits or 16-bits wide. This new control signal is labeled sXTRQ*. It is on bus line 58 and it is pulled "low" whenever the 16-bit CPU wants to perform a 16-bit transfer. With the 8/16 RAM, an acknowledging signal, SXTN* (bus line 60) is sent back to the CPU telling it that a 16-bit transfer is possible. (Our 8086 CPU is capable of transferring "two gulps" of 8-bit data if this acknowledgement is not received. Thus, older 8-bit only RAMs can be used with our 8086 CPU board, although at a significant loss in speed.)

The addition of the 16-bit mode of data transfer on the S-100 bus requires the control circuity on the new generation of RAM boards like our 8/16 to become more sophisticated. How the 8/16 RAM decodes the CPU control signals to determine whether the data coming into the RAM board will be on the Data In or Data Out bus and which bus should receive the data read will be discussed later in this section.

SCHEMATIC SHEET 1

It is suggested you locate schematic sheet one and follow along as the board's operation is discussed.

This sheet contains the:

1. Memory Array

2. Data In and Data Out Buffers

* Indicates an active low signal.

MEMORY ARRAY

To accommodate 16-bit transfers to and from memory and the switching which must be done between the Data In and Data Out busses, the memory array is divided into an "even" and an "odd" section. The 16 memory chips at the top of the array (U18 through U2F) store only odd-addressed data. The 16 lower memory chips (U10 through U27) store only even-addressed data.

The address lines A-1 through A-16 are connected in parallel to all 32 chips in the memory array. MWRITE (after buffering) is also connected to all 32 memory chips. Note that A-0 is not connected directly to the memory chips. A-0 is used as a control signal which helps determine if the data transfer should be with the "odd" or "even" section of the array.

The chip select lines -- CSA*, CSB*, CSC*, and CSD* -- are generated by circuitry contained on sheet two of the schematic and will be discussed later.

DATA IN AND DATA OUT BUFFERS

The memory board has six sets of data buffers. All use 74LS240 ICs which offer Schmit trigger inputs for high noise immunity and high drive for signal sourcing. The chart below shows when these buffers are enabled to put the correct data on the correct bus.

Data Buffer Enabling Signals

Function	Address: even or odd	Buffer Enable Signals Active
8-bit Read	even	ENB*
8-bit Read	odd	ENC*
16-bit Read	even address only	ENA*, ENC*
8-bit Write	even	none required
8-bit Write	odd	A-0 (Note 1)
16-bit Write	even address only	A-0 (Note 2)

Note 1: A-0 on the bus is "high".

Note 2: A-0 on the bus is "low".

How these data buffer enabling signals are generated will be shown on sheet two of the schematic.

* Indicates an active low signal.

SCHEMATIC SHEET TWO

This sheet contains the circuits for:

1. Address buffers
2. MWRITE Buffer
3. Extended Address Decoder
4. Address Decoding
5. Data In -- Data Out Buffer Enabling
5. Chip Select Signal Generation
6. Data In -- Data Out Buffer Enabling
7. Power Supply

Each will be discussed in turn.

ADDRESS BUFFERS

All address signals, A-0 through A-23, are buffered by 74LS240 or 74LS244 Schmit trigger buffers. Their hysterisis inputs provide high noise immumnity for the information contained on these lines. (Note: all signal inputs to the 8/16 memory card are Schmit trigger buffered.)

The address buffer outputs for lines A-1 through A-12 go directly to the memory array where they feed all 32 memory chips.

MWRITE BUFFER

The MWRITE signal is buffered and sent to all 32 chips in the memory array. Note, however, no writing action can take place unless the MWRITE signal and the chip select signal are active at the same time. During a read operation, the MWRITE signal is not active.

EXTENDED ADDRESS DECODING

This circuit's purpose is to disable or partially enable the memory board, depending upon the information contained on address lines A-16 through A-23. For the board to be enabled, among other things) the outputs of the two 74LS136 EXOR comparators must be high. This only occurs when the two inputs to each of the eight gates differ from one another. For any setting of the extended address switches, there is only one combination of A-16 though A-23 signals which will result in a high level signal at the output of the gates. How these switches are set is described earlier in this manual under "addressing".

Note that the board can be caused to ignore the extended address by opening the "Extend Enable" switch (segment 5 of S-2).

ADDRESS DECODING

U39, a 74LS283 adder, is used to compare the address set into the "Board Address" switches (segments 1 through 4 of S-2) with the address information contained on the bus lines representing A-12 through A-15. The adder is so connected that output pins 13 and 10 will both be "high" for a 16K block beginning with the address selected. (See the chart under "addressing" for switch settings for various board addresses.)

CHIP SELECT SIGNAL GENERATION

Chip Select is a function of:

1. Has the board been selected by the address (is the output of U-38 low?)

2. A-0 (should the even or odd section of the array be selected?)

3. A-13 (most significant address bit for the array.)

4. Has and active sXTRQ* signal been received?

To result in an active (low)	CSA*	CSB*	CSC*		CSD*	
Output of U38 is:	low	low	low	low	low	low
A-13 is:	high	low	high	high	high	high
A-0 is:	low	low	high	X	high	X
SXTRQ* is:	high	high	X	low	X	low

(X indicates "don't care" state)

DATA IN -- DATA OUT BUFFER ENABLING

The read buffers are enabled by:

ENA* -- Used for 16-bit reads only

ENB* -- Used for an 8-bit read of and EVEN address

ENC* -- Used for an 8-bit read of and ODD address or
used for a 16-bit read

For ANY of these read buffers to be enabled:

This particular board must be enabled at the current address (the output of U-38 is low), and

pDBIN must be high (read control signal)

For selection of WHICH read buffer is enabled:

A-0 selects the "even" or "odd" array

sXTRQ* being active selects a 16-bit read

The write buffers are enabled by:

A-0 only (is address even or odd?)

Note: Write buffer U-40 is always enabled. Both 8-bit and 16-bit "writes" use this path.

POWER SUPPLY

The power supply consists of four nearly identical circuits. Considering the one containing U49, C-1 prevents oscillation of the regulator while C-5, C-9, C-13, C-10, C-14, C-11, C-12, and C-15 provide transient suppression.

Trouble-Shooting

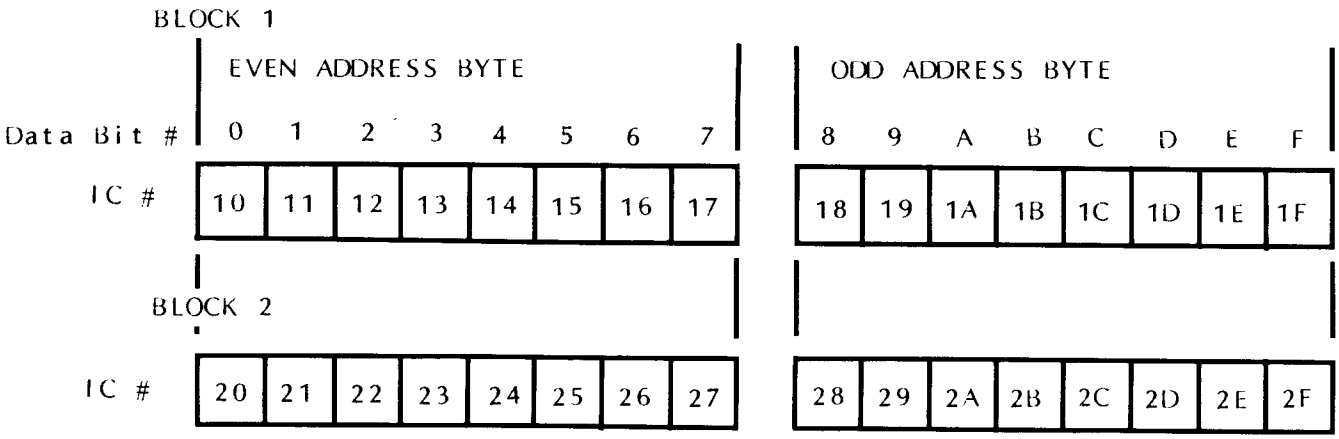
Most memory tests will detect a fault if it exists on the 8/16 memory board. However, some tests may not issolate this fault to a single memory chip. An example of this can be seen while testing this board with the Seattle Computer Products Static RAM Tester. This tester isolates memory chip faults only to a 1K block. Because the 8/16 memory array is "interleaved", that is, the even address data is stored in one chip while the odd address data is stored in another, the tester will issolate memory chip faults to two possible defective chips. Substitution will have to be used to determine which of the two is actually defective.

Any memory test which isolates to an absolute address will exactly define a bad chip in the 8/16 memory array.

MEMORY ARRAY ORGANIZATION

The organization of the memory array and the method of selecting memory chip IC numbers is not obvious for the 8/16. This is because of the need for the memory array to appear to be 8 bits wide (one byte) for 8-bit transfers and 16 bits wide (two bytes) for 16-bit transfers.

To understand the organization, it is convenient to think of the array as being composed of two blocks, each consisting of words 16 bits wide (two 8-bit bytes) and 4K deep. See the diagram below:



Normally, while running a program, memory cells are selected in sequence. If 16-bit transfers are being used, the program counter will step the memory address two bytes per increment (always using the even address). If 8-bit transfers are called for, the counter will increment the memory address one byte at a time.

Referring to the diagram, you will see that for a normal 8-bit read transfer sequence, data will be selected from perhaps the even address cell, then the next byte will be from the odd address, then even, odd, even, . . . each succeeding access alternating between even and odd memory addresses. With the access alternating between memory chips, the chips are said to be "interleaved".

MEMORY CHIP IDENTIFICATION

The previous diagram will allow you to associate a particular memory chip with a specific address. Assuming the memory board is addressed to start at 0000H, block 1 runs from 0000H to 1FFFH and block 2 runs from 2000H to 3FFFH.

One-Year Limited Warranty

WARRANTEE AND WARRANTY PERIOD

The Seattle Computer Products (hereinafter referred to as SCP) warranty for this product extends to the original purchaser and all subsequent owners of the product for a period of one year from the time the product is first sold at retail and for such additional time as the product may be out of the owner's possession for the purpose of receiving warranty service at the factory.

WARRANTY COVERAGE

This product is warranted to be free from defects of material and workmanship and to perform within its specifications as detailed in the instruction or operating manual during the period of the warranty.

This warranty does not cover damage and is void if the product has been damaged by neglect, accident, unreasonable use, improper repair, or other causes not arising out of defects in material or workmanship.

WARRANTY PERFORMANCE

During the warranty period, SCP will repair or replace defective boards or products or components of boards or products upon written notice that a defect exists. Certain high value parts may have to be returned to SCP prior to replacement. Other components will be replaced without the part having to be returned to the factory with the exception the SCP retains the right in all cases to examine the defective board or other products prior to the items replacement under the warranty. In the event the return of the board, product, or component is requested by SCP under this warranty, the owner shall ship the item prepaid to the SCP factory. SCP will pay for shipment of replacement items back to the owner. All repairs or replacements under this warranty will be performed by SCP within five working days of receipt of notice of defect or return of components as called for under this warranty.

WARRANTY DISCLAIMERS

While high reliability was a major design factor for this product and care was used in its manufacture, no certainty can be achieved than any particular product will operate correctly for any specific time. No representation is made by SCP that this product will not fail in normal use. Because of the inability to guarantee 100% reliability, SCP shall not be liable for any consequencial damange the user may suffer because the products fails to function reliably 100% of the time. Any implied warranties arising from the sale of this product are limited in duration to the warranty period defined above.

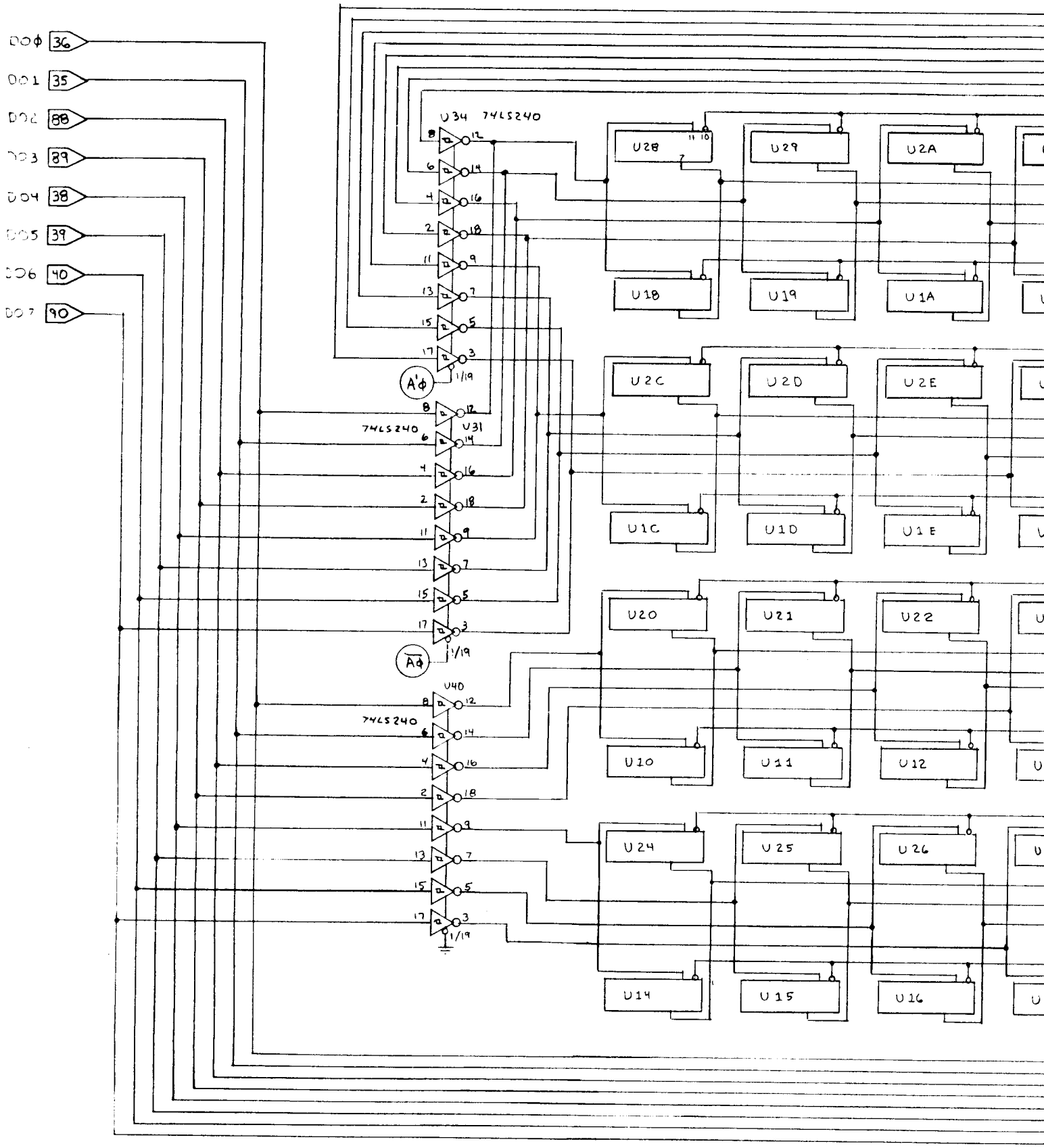
LEGAL REMEDIES

This warranty gives the purchaser specific legal rights. He may have additional rights which vary from state to state.

SHIPPING INSTRUCTIONS

In the event it becomes necessary toreturn the product or component to SCP, also return a written explaination of the difficulty encountered along with your name, address and phone number. Package the items in a crushproof container with adequate packing material to prevent damage and ship prepaid to:

Seattle Computer Products
1114 Industry Drive
Seattle, Washington 98188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D01 35
D02 88
D03 89
D04 38
D05 39
D06 40
D07 90
U34 74LS240
U31 74LS240
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A'Φ
AΦ
U28
U29
U2A
U18
U19
U1A
U2C
U2D
U2E
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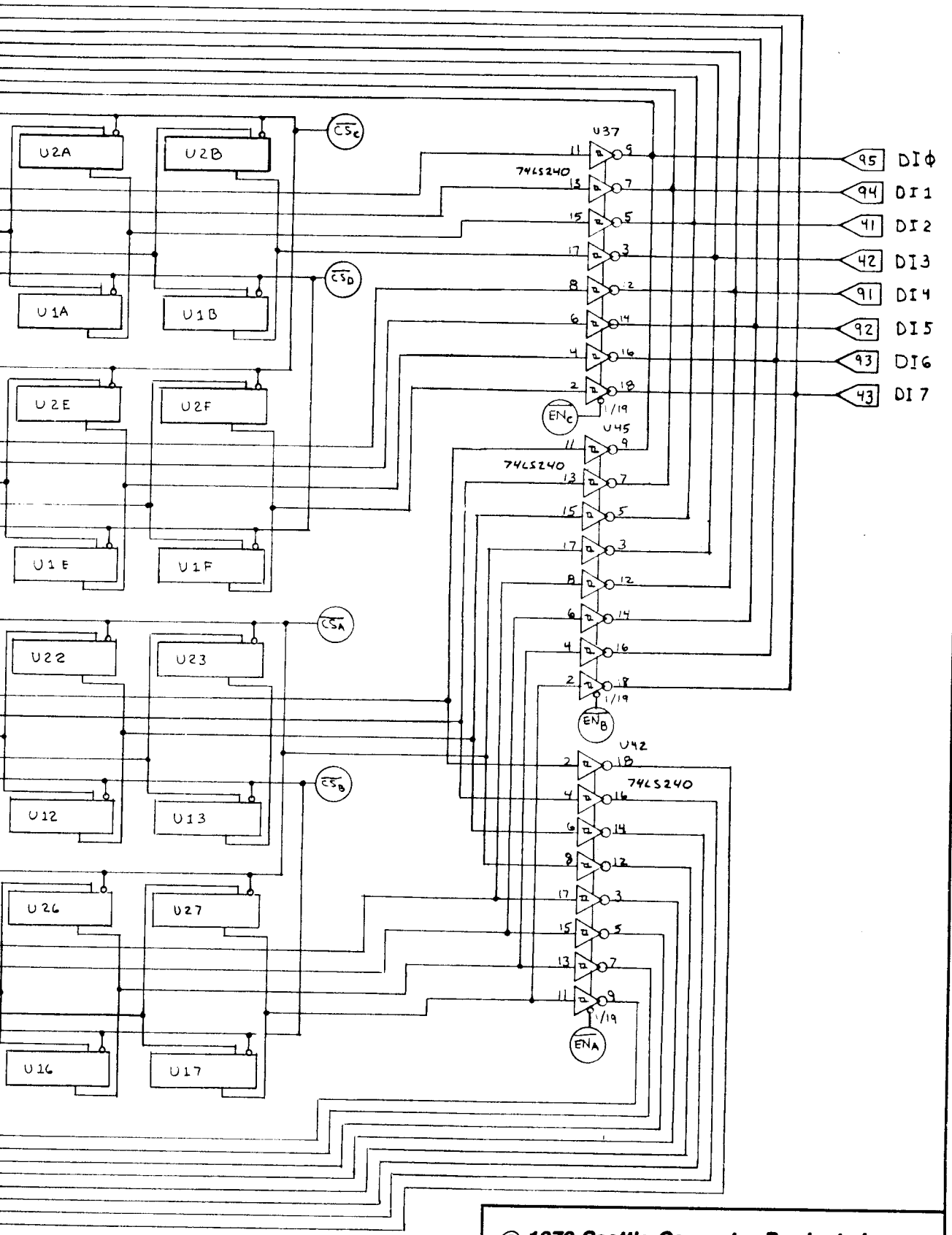

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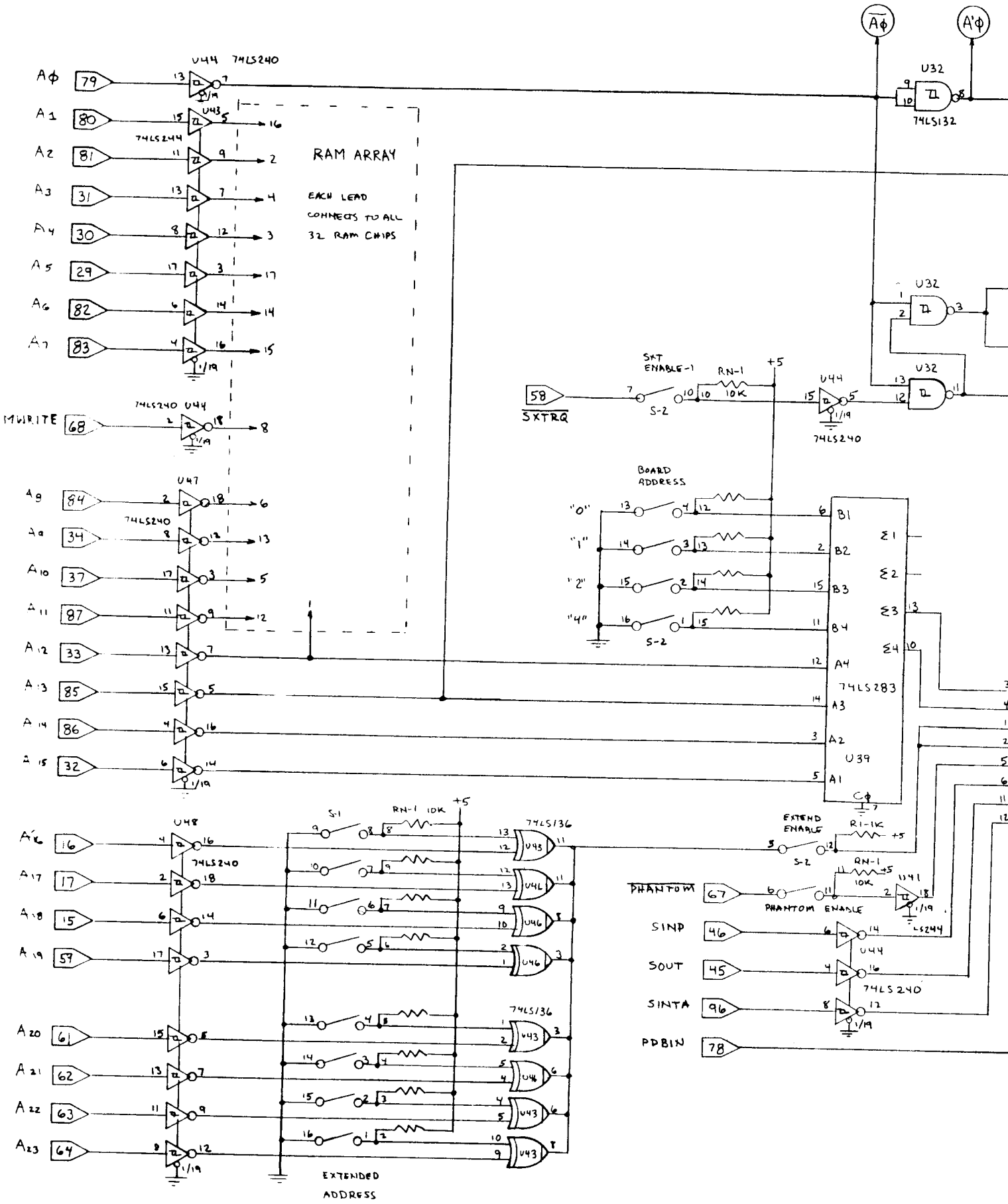

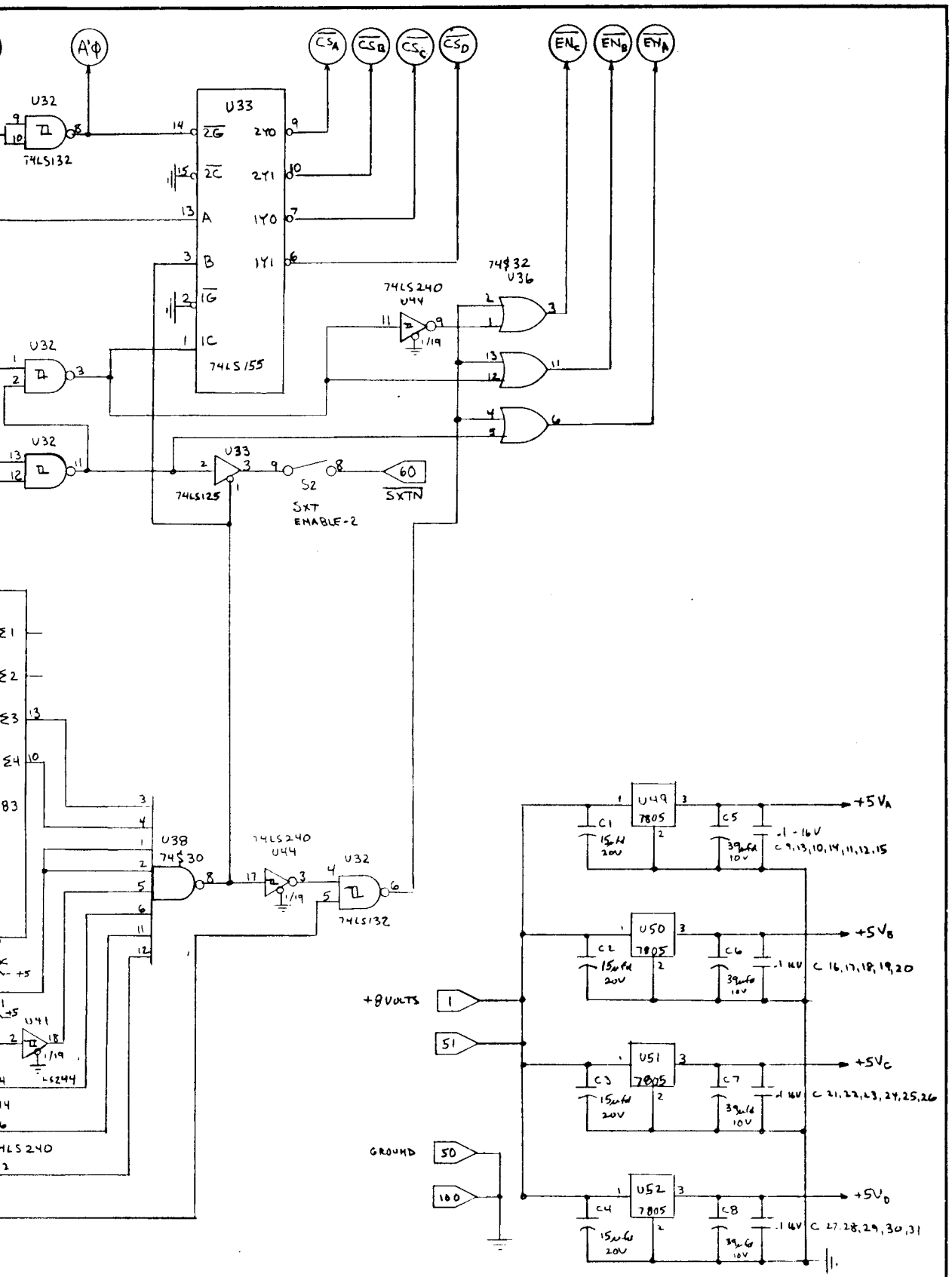

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SCHEMATIC – 8/16 RAM

SHEET 2 OF 2

DRAWING NUMBER SCP 107A